WHAT IS CLAIMED IS:

1. A semiconductor comprising:

a substrate having a semiconductor layer;

an element isolating insulating film for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film being formed on said substrate so as to penetrate said semiconductor layer and having a top surface projecting upward above a surface of said semiconductor layer; and

A MOS type element formed within a corresponding one of the element regions and having a gate insulating film, wherein:

a difference in height from the substrate between the top surface position of said element isolating insulating film and the top surface position of said semiconductor layer is at least three times as large as the thickness of said gate insulating film.

2. A semiconductor device comprising:

a substrate having a semiconductor layer;

an element isolating insulating film for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film being formed on said substrate so as to penetrate said semiconductor layer and having a top surface projecting upward above a surface of the semiconductor layer; and

A MOS type element formed within a corresponding one of said element regions, wherein:

a difference in height from the substrate between the top surface position of the semiconductor layer and the top surface position of the element isolating insulating film is at least 10 nm.

3. A semiconductor device comprising:

a substrate having a semiconductor layer;

an element isolating insulating film for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film being formed on said substrate so as to penetrate said semiconductor layer and having a top surface projecting upward above a surface of the semiconductor layer; and

A MOS type element formed within a corresponding one of said element regions and having a gate insulating film and a metal gate electrode formed thereon, wherein:

said gate insulating film and said metal gate electrode are formed on a top surface and sides of the semiconductor layer in said element region which are not covered with said element isolating insulating film.

4. A semiconductor device according to claim 3, wherein the difference in height from said substrate between the top surface position of said semiconductor

layer and the top surface position of said element isolating insulating film is at least five times as large as a thickness of said gate insulating film.

5. A semiconductor device according to claim 3, wherein the MOS element includes a source/drain region and the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is substantially at least a junction depth of said source/drain region.

6. A semiconductor device comprising:

a semiconductor substrate having on its surface a recess and at least one projection formed in the a recess, the projection having a channel region;

an element isolating insulating film formed in the said recess

a MIS type semiconductor element formed on said semiconductor substrate and including a gate electrode formed on said channel region of said projection via a gate insulating film, and a source and a drain regions formed to pinch said channel region of said projection therebetween, wherein:

a channel region of said MIS type semiconductor element is formed to reach said at least one projection located adjacent to the MIS type semiconductor element in its channel width direction via said recess, and a top surface of said at least one projection is located

higher than the top surface of said element isolating insulating film.

7. A semiconductor device comprising:

a semiconductor substrate having a recess and projections formed on its surface;

an element isolating insulating film formed in said a recess and having its top surface located below top surfaces of said projections; and

a MIS type semiconductor element using a region of said semiconductor substrate as a channel region and including a gate electrode formed on said channel region via a gate insulating film, and a source and a drain regions formed to pinch said channel region therebetween, wherein:

said channel region of said MIS type semiconductor element is divided into at least two sections in the channel width direction by means of said element isolating insulating film and has first regions near steps between said recesses and said projections and second regions corresponding to the projections between the first regions, and

$W_i - W_t > G_t$ where G_t denotes the sum of the widths of said a recess in the channel with direction, W_t denotes the sum of the widths of said projections in the channel with direction, and W_i denotes an assumed channel width of an assumed semiconductor element in which its channel width is equal to that of the MIS

type semiconductor element, in which the current density of a current through its channel region is equivalent to that of a current through the second regions of said MIS type semiconductor element, and in which the total current through its channel region is equivalent to that through the channel region of said MIS type semiconductor element.

8. A semiconductor device according to claim 6, wherein the top surface of said isolating insulating film is formed deeper than portions of said source and drain regions near said gate electrode.

9. A semiconductor device according to claim 7, wherein the top surface of said isolating insulating film is formed deeper than portions of said source and drain regions near said gate electrode.

10. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a semiconductor substrate;

forming openings in said insulating film to partly expose a surface of said semiconductor substrate;

using the exposed portion as a seed to epitaxially grow and form a semiconductor layer of thickness sufficient to fill said openings and to extend upward above said insulating film; and

removing portions of said semiconductor layer outside said openings.

11. A method for manufacturing a semiconductor device comprising the steps of:

forming a monocrystalline insulating film on a semiconductor substrate;

forming a non-monocrystalline insulating film on said monocrystalline insulating film;

forming openings in said non-monocrystalline insulating film to partly expose a surface of said semiconductor substrate;

using the exposed portion as a seed to epitaxially grow and form a semiconductor layer of thickness sufficient to fill said openings and to extend upward above said insulating film; and

removing portions of said semiconductor layer outside said openings.

12. A method for manufacturing a semiconductor device according to claim 10, further comprising the step of making a top surface of said semiconductor layer within said openings lower than an opening surface of each of said openings.

13. A method for manufacturing a semiconductor device according to claim 11, further comprising the step of making a top surface of said semiconductor layer within said openings lower than an opening surface of each of said openings.

14. A method for manufacturing a semiconductor device according to claim 12, wherein the top surface

of said semiconductor layer within said openings is made lower than the opening surface of each of said openings by selectively etching said semiconductor layer within said openings or oxidizing a top portion of said semiconductor layer within said openings and selectively removing the oxidized portion.

15. A method for manufacturing a semiconductor device according to claim 12, wherein the top surface of said semiconductor layer within said openings is made lower than the opening surface of each of said openings by selectively etching said semiconductor layer within said openings or oxidizing a top portion of said semiconductor layer within said openings and selectively removing the oxidized portion.

16. A method for manufacturing a semiconductor device according to claim 12, further comprising the step of heating said semiconductor layer in an inert gas atmosphere after the step of making the top surface of said semiconductor layer within said openings lower than the opening surface of each of said openings.

17. A method for manufacturing a semiconductor device according to claim 13, further comprising the step of heating said semiconductor layer in an inert gas atmosphere after the step of making the top surface of said semiconductor layer within said openings lower than the opening surface of each of said openings.

18. A method for manufacturing a semiconductor

device according to claim 10, wherein the portions of said semiconductor layer outside said openings are removed by means of chemical mechanical polishing or mechanical polishing.

19. A method for manufacturing a semiconductor device according to claim 11, wherein the portions of said semiconductor layer outside said openings are removed by means of chemical mechanical polishing or mechanical polishing.

20. A method for manufacturing a semiconductor device according to claim 12, wherein the portions of said semiconductor layer outside said openings are removed by means of chemical mechanical polishing or mechanical polishing.

21. A method for manufacturing a semiconductor device according to claim 13, wherein the portions of said semiconductor layer outside said openings are removed by means of chemical mechanical polishing or mechanical polishing.

22. A method for manufacturing a semiconductor device according to claim 10, wherein after the step of forming said semiconductor layer, a semiconductor film is formed all over the surface thereof, and in the step of removing the portions of said semiconductor layer outside said openings, said semiconductor film is also removed.

23. A method for manufacturing a semiconductor

device according to claim 11, wherein after the step of forming said semiconductor layer, a semiconductor film is formed all over the surface thereof, and in the step of removing the portions of said semiconductor layer outside said openings, said semiconductor film is also removed.

24. A method for manufacturing a semiconductor device according to claim 12, wherein after the step of forming said semiconductor layer, a semiconductor film is formed all over the surface thereof, and in the step of removing the portions of said semiconductor layer outside said openings, said semiconductor film is also removed.

25. A method for manufacturing a semiconductor device according to claim 13, wherein after the step of forming said semiconductor layer, a semiconductor film is formed all over the surface thereof, and in the step of removing the portions of said semiconductor layer outside said openings, said semiconductor film is also removed.

26. A method for manufacturing a semiconductor device according to claim 10, wherein said insulating film is a laminated film including a silicon oxide film and a silicon nitride film formed thereon, and after the silicon nitride film has been formed on side walls of each of said openings, a silicon layer is formed as said semiconductor layer.

27. A method for manufacturing a semiconductor device according to claim 11, wherein said insulating film is a laminated film including a silicon oxide film and a silicon nitride film formed thereon, and after the silicon nitride film has been formed on side walls of each of said openings, a silicon layer is formed as said semiconductor layer.

28. A method for manufacturing a semiconductor device according to claim 12, wherein said insulating film is a laminated film including a silicon oxide film and a silicon nitride film formed thereon, and after the silicon nitride film has been formed on side walls of each of said openings, a silicon layer is formed as said semiconductor layer.

29. A method for manufacturing a semiconductor device according to claim 13, wherein said insulating film is a laminated film including a silicon oxide film and a silicon nitride film formed thereon, and after the silicon nitride film has been formed on side walls of each of said openings, a silicon layer is formed as said semiconductor layer.

30. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a semiconductor substrate;

forming openings in said insulating film to partly expose a surface of said semiconductor substrate;

using the exposed portion as a seed to epitaxially grow and form in said openings a semiconductor layer that is not thick enough to reach an opening surface of each of said openings; and

heating said semiconductor layer in an inert gas atmosphere.

31. A method for manufacturing a semiconductor device according to claim 10, wherein said inert gas atmosphere contains hydrogen.

32. A method for manufacturing a semiconductor device according to claim 11, wherein said inert gas atmosphere contains hydrogen.

33. A method for manufacturing a semiconductor device according to claim 30, wherein said inert gas atmosphere contains hydrogen.